摘要

本論文提出以 HDL（硬體描述語言）爲基礎的設計方式來實現可程式計數器／計時器.選擇英特爾 8254 晶片作爲定義該可程式計數器／計時器的功能和規格.VHDL 首次用來作爲發展 8254 的工具,並藉由使用 ModelSim 來驗證其功能的正確性.再透過合成其硬體電路加以分析.基於本文所提出以 VHDL 爲基礎的設計方式,可從實驗結果顯示,具有高複雜度的可程式計數器／計時器可以快速且符合成本效益的加以實現.

關鍵字：VHDL, 可程式計數器／計時器

Introduction

As digital system becomes more and more complex, it becomes very difficult to design the system using the traditional logic design approach. Furthermore, for complex digital system design, it has become increasingly important to verify the functionality of the design before implementation[1]. HDL is becoming very popular because it can be used for design, simulation, synthesis, and testing of digital systems.

The United States Department of Defense developed VHDL in 1982.VHDL describes the behavior, function, inputs, and outputs of a digital circuit design. VHDL has become a well-known language for digital system design and is in widespread use today.

A programmable counter/timer(PCT) has wide applications in microcomputer I/O and data acquisition systems. PCT is used to count the occurrences of a digital event or digital pulse, and generate pulses or square waves output. PCT can generate accurate time delays under software control.