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# 以 VHDL 設計可程式〝計數器/計時器〞

# Design of Programmable Counter/Timer Using VHDL

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**Abstract**

A programmable counter/timer based on HDL (Hardware Description Language) design is proposed.The Intel 8254 is selected for defining the functionality and specifications of the programmable counter/timer.VHDL programs are first eveloped to emulate the functional operation of 8254.Next,the programs are verified by simulation using ModelSim.Then the hardware circuit is synthesized and analyzed.The experimental results show that,based on the proposed VHDL-driven design,a high complexity programmable counter/timer can be realized by programmable logic quickly and cost-effectively.

Keywords：VHDL, FPGA, COUNTER/TIMER