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VLSI ARCHITECTURE

FOR SERIAL INPUT CLUSTERING ANALYSIS

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Abstract

Clustering analysis has numerous applications in image processing and pattern recognition. The squared error clustering algorithm is the most well-known method in clustering analysis. VLSI implementation of the squared error clustering algorithm is feasible recently due to advances in microelectronics technology. This paper presents a modular serial input VLSI architecture for the squared error clustering analysis based on systolic array. The proposed architecture features simple, regular and modular design which dramatically reduces the circuitcomplexity. Moreover, the proposed architecture can be utilized for adaptation to the change of the number of input patterns. In addition, the proposed architecture allows serial data input to save enormous pin counts, which is very attractive for VLSI implementation. Using this novel architecture, the VLSI implementation for clustering analysis can be realized cost-effectively.

I. INTRODUCTION

Clustering analysis is a valuable technique in unsupervised data analysis, especially when limited prior information about the given data set is known [1]. The clusters obtained from clustering analysis have the result that patterns in the same cluster are more similar than patterns belonging to different clusters [2]. The results of clustering analysis are used to find natural grouping in a data set, which helps the user understand the structure or property of the data